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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,476	02/10/2004	Wayne A. Locb	MP0351	4057

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EXAMINER	
JACKSON, BLANE J	
ART UNIT	PAPER NUMBER
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,476	LOEB ET AL.	
	Examiner	Art Unit	
	Blane J. Jackson	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,6-8,13-18,23,25 and 29-79* is/are allowed.

6)☐ Claim(s) *4,9-11,19-22,24 and 26-28* is/are rejected.

7)☒ Claim(s) *2,3,5 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Upon review of the After Final Amendment filed 25 January 2007, the examiner found a new grounds of rejection for claims 9 and 26 and associated dependent claims. Consequently, a Non-Final Rejection follows to address the claims. The amendment to claims 1, 6-8, 13-18, 23, 25, 29-40, 42-44 and 46-79 placed them in condition for allowance. Claims 41 and 45 remain in condition for allowance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 9-11, 19-22, 24 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldfarb et al. (US 6,400,227) in view of Klaren et al. (US 2004/0095190).

As to claims 9 and 26, Goldfarb teaches a circuit comprising:

Means for *coupling an analog signal to provide a first coupled signal* (figure 1, column 2, lines 31-67, the signal input to the variable gain amplifier is suitably coupled via coupling capacitor (C7)),

Means for providing an adjustably amplified output from said first coupled signal (column 2, lines 37-60, parallel branches comprising an amplifier having at least two FETs connected in a cascode configuration where each parallel branch the gate of the common gate FET is coupled through an isolation resistor to a gain control input),

Means for selecting an output power range for said adjustably amplified output (column 2, lines 47-60, each of the gain control inputs (VGC1-VGC4) are activated or disabled by a control circuit to enable a desired combination of branches and thus a desired gain level),

Means for providing a bias signal comprising a current mirror and a means for providing a current to said current mirror (figure 1, column 4, lines 1-25, bias points for FETs (1, 3, 5 and 7) are controlled by the bias current (Ibias) via current mirror FET (12)).

Goldfarb teaches means for coupling an analog signal to provide a first coupled signal to the input of the plurality of parallel adjustable power amplifier but is silent as to means for amplifying an analog signal to provide a first amplified signal.

Klaren teaches a power amplifier (figure 1) comprising two parallel amplifiers (38 and 40) that are preceded by an amplifier driver stage (22) where both the driver and power amplifiers are under bias control for gain control, paragraphs 0040-0045. Klaren, though primarily focused on methods to bypass the PA package, also demonstrates a fixed driver amplifier (132) to amplify an analog signal and provide a first amplified output at a common node, the node represented by the band pass filter (134) prior to signal splitting at the quadrature hybrid (152), figure 7, paragraphs 0008 and 0015.

Since Klaren teaches an amplifier driver, band pass filter and hybrid as known components to precede the actual parallel adjustable power amplifiers of a power amplifier package, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the coupling circuit of Goldfarb to include the driver amplifier of Klaren to meet design signal drive levels to the adjustable power amplifier.

As to claims 10 and 27 with respect to claims 9 and 26, Goldfarb teaches the circuit wherein said means for providing said bias signal further comprises a means for buffering an output from said current mirror (figure 1, column 4, lines 1-25, current mirror FET (12) sets a controlled DC bias voltage level through isolation resistor (R10) to the gates of FET1, FET3, FET5 and FET7).

As to claim 11, Goldfarb teaches the adjustable amplifier of claim 9 further comprising a current source (figure 1, column 4, lines 1-11, precise bias control using bias current Ibias and current mirror FET (12)).

As to claim 19 with respect to the circuit of claim 26, Goldfarb teaches wherein said means for providing said adjustably amplified output comprises a plurality of parallel, independently selectable means for further amplifying said first amplified signal, each of said parallel means for further amplifying having an input at a first common node and an output at a second common node (figure 1, column 2, lines 31-60).

As to claim 20 with respect to the circuit of claim 19, Goldfarb teaches said adjustably amplified output has one of a plurality of power ranges corresponding to a number of selected means for further amplifying, said output signal having a minimum power efficiency when two or more of said means for further amplifying are selected (column 3, line 10 to column 4, line 25, transconductance ratios of 4:4:2:1 determined for the four parallel power amplifiers producing typical bias currents of 2 ma for the first and second branches, 1ma for the third branch amplifier and 0.5 ma for the fourth branch amplifier enabling the correct combination of amplifiers for the desired output power such that the DC current is reduced as output power is reduced to improve battery life).

As to claim 21 with respect to claim 20, Goldfarb teaches having a power efficiency of at least 50% of a maximum efficiency of said circuit (column 4, lines 13-25, bias may be set to any particular operating class or design and selected upon system requirements such as output power, linearity or efficiency).

As to claim 22 with respect to claim 19, Goldfarb teaches each of said means for further amplifying comprises a transistor having a control terminal and said circuit further comprises a first means for coupling said control terminal of at least on of said transistors to a first bias (figure 1, column 4, lines 1-11, bias control which maintains the individual or common bias points coupled to the branch amplifiers for FETs (1, 3, 5 and 7) via a respective series resistor (RS, R4, R5 and R6)).

As to claims 4 and 24 with respect to claims 9 and 19, Goldfarb teaches each of said means for further amplifying comprises a transistor having a control terminal and a first means for coupling said control terminal of said transistor to a bias signal (figure 1, column 2, lines 47-60, selected isolation resistors (R3, R4, R5 and R6) couple the control signal (VGC1-4) to a respective control terminal of FET2, FET4, FET6 and FET8).

As to claim 28, Goldfarb teaches the circuit of claim 19 wherein at least one of said plurality of means for further amplifying is selected for operation (figure 1, column 2, lines 47-60, desired combination of branches are selected for a corresponding desired gain level).

Claim 80 is cancelled.

Allowable Subject Matter

Claims 1, 6-8, 13-18, 23, 25 and 29-79 are allowed. As to claims 1, 18 and 65, the prior art teaches an adjustable segmented amplifier comprising a plurality of independently selectable parallel amplifier segments comprising a transistor having a control terminal but does not teach each parallel amplifier segments also comprises a first inductor configured to resonate with a capacitance at a base of the transistor and in electrical communication with a control terminal of the transistor.

As to claims 41 and 45, the prior art made of record teaches a system for broadcasting an analog signal comprising an integrated circuit and an output inductor coupled to a second common output node of an adjustable stage comprising a plurality of independently selectable parallel amplifier segments but does not teach an adjustable resistor coupled to the output inductor.

As to claims 70 and 71, the prior art made of record teaches a method of amplifying an analog signal comprising selecting one or more parallel amplifier segments, each segment comprises a transistor having a control terminal but does not teach an each of the parallel amplifier segments also comprises a first inductor in electrical communication with the control terminal of the transistor.

Claims 2, 3, 5, 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. As to claims 2, 3 and 5, the prior art made of record does not teach an adjustable stage comprises a first inductor in electrical communication with said control terminal of at least one of said transistors.

As to claim 12, the prior art made of record teaches the current source comprises a FET but does not teach the current source comprises a programmable digital to analog converter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Thursday, 7:30 AM-6:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.